A Virtual DSP System for Design Instruction of Power Converters

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Abstract: This paper describes the development of an object oriented DSP based for design and control of power converters. The testbed is developed using a Texas Instrument digital signal processing (DSP) chip for a hardware-in-the-loop simulation system. The system consists of object-oriented Windows-based software written in C++ and a controller hardware system for rapid prototyping and easy testing of different control algorithms. It is shown that the custom virtual test bed developed presents some advantages over conventional simulation software packages. The concept developed in this paper can also be applied for different types of resonant converters or other power electronics systems.
Keywords: resonant power converters, simulation, virtual test bed, digital signal processing.

I. INTRODUCTION

In this paper a resonant power converter is used as a case study for the development of the testbed. The resonant power converters provide efficient electric power transfers required in many industrial, aerospace, and automotive applications. Unlike the usual 'hard' switching power converters, a resonant converter utilizes a controlled series or parallel LC resonant circuit to achieve zero current and/or zero voltage switching ('soft' switching) which substantially reduce the switching losses occurred in the power transfer process

Despite their attractiveness, most resonant converters require complex control circuitry and timing requirements. Moreover, the control strategy employed to achieve certain power transfer objectives is highly dependent on the type of loads being used and applications. These difficulties have led to the need for a development framework that allows system designers to test and evaluate different control strategies specific for their applications.

In this paper, the design and development of a virtual test bed system for a type of resonant converter is discussed. The test bed system is configured so that it matches the actual hardware implementation as close as possible, allowing the system to be used as a 'virtual test bed' for the actual hardware development. To achieve this objective, controller hardware has been included in the virtual test bed to allow direct implementation of control algorithms on the chosen controller architecture.

The test bed system is designed using Object Oriented Approach and implemented on a Windows-based PC using the native C++ language. Despite the wide availability of general simulation packages such as MATLAB, Simulink, SPICE, or SABER, the authors have chosen to develop the test bed system using a custom written software, for the following reasons :

- *Speed*
  The use of the compiled PC native C++ codes removes the unnecessary software overhead associated with the interpreted script language commonly available in general simulation packages such as MATLAB or Simulink.

- *Flexible computation accuracy*
  The virtual test bed system is intended to be used for control algorithms development rather than as circuit performance evaluator. For this reason, unnecessary accurate circuit devices models such as those provided in SPICE or SABER can be avoided to achieve faster simulation time. The integration methods and circuit devices modeling can be chosen flexibly to yield in the required accuracy.

- *True object oriented approach for design and implementation.*
  The C++ language allows for the design and implementation of the test bed system using a true object oriented approach. Compared to simulation package such as Simulink MATLAB that offers block diagrams approach the object-oriented approach to simulation is superior in certain aspect [6]. The object-oriented approach allows for better system partitioning and visualization in solving complex system. Moreover C++ code is relatively easy to maintain, reuse, and modify and allow for a group of programmers to work on separate parts of the code, without the errors multiplying in proportion to the length of the code. Programs written in C++ can be maintained and extended more easily and addition of functionality to the code is relatively straightforward with fewer risks of introducing errors. By using object oriented features, such as inheritance, reusing already written code is made more practical and

codes comparable to Fortran in efficiency can in fact be written in C++, along with the added benefits of saving valuable implementation time due to ease of code re-usability and maintenance [7].

- *Availability of C++ visual programming packages.*
  Nowadays, visual programming packages for C++ are widely available that can save considerable amount of time in designing and implementing graphical user interface for the test bed. The test bed developed in this paper has been developed using the Borland C++ Builder compiler that offers visual programming for C++ running on PC with Windows 95/NT [8,9].

- *Cost*
  The cost of a general simulation packages far exceed even a full featured C++ compiler.

II. THE UNIPOLAR SERIES RESONANT CONVERTER

In the past several years, many research projects have been conducted in resonance power converters [1-4]. Notable among these are the *unipolar series resonance converters* also known as the *DC-Link Current Converters*. This type of resonant converter performs the power transfer from the input to the output through the generation of a train of current pulses called link current. The term "unipolar series" is used to denote the fact that the link current flows in only one direction through a resonance LC tank placed in series with the load. The unipolar nature of the link current is desirable in this case, for it allows the use of relatively less expensive unidirectional switches such as thyristors. Fig. 1 shows a block diagram of a unipolar series resonance converter for a 3-phase input and 3-phase output system, which has been used in the virtual test bed.

The Link Current Generator block shown in Fig. 1 generates the unipolar link current pulses. One of the features of the unipolar series resonant converter is that the link current is generated in such a way so that all the turning on/off of the power switches occur at substantially zero voltage (ZVS = Zero Voltage Switching) and/or zero current (ZCS = Zero Current Switching). These conditions result in substantially reduced switching losses compared to a conventional hard switching power converter.

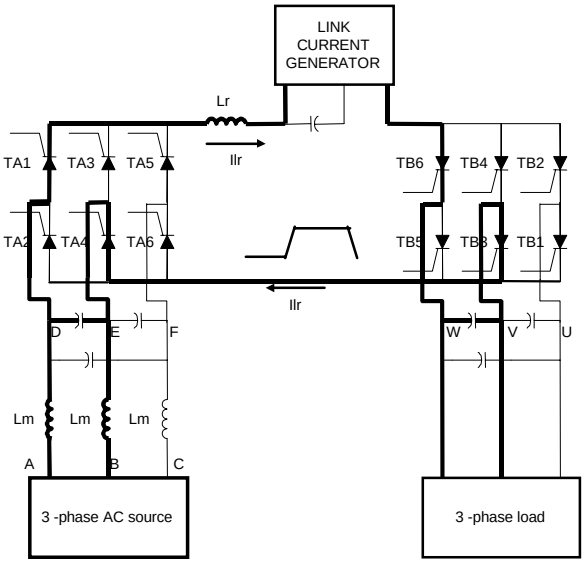

Fig. 1 USRC as a 3 phase input and 3 phase output system

2.1 Link Current Generation

Researches in the dc link converters for the past several years have been oriented towards achieving a square-wave-like link current waveform with as greater control of its amplitude and duty cycle as possible [5]. The square wave-like waveform is desirable since it permits less peak current to support certain load requirement compared to a sinusoidal-like waveform.

Many link current generator circuit topologies have been proposed in order to achieve the above goals [3-5]. One of them, which has been adopted for the virtual test bed system is shown in Fig. 2 [1].

The desired square wave-like link current is generated through selectively choosing active resonance circuit modes formed when combination of switches in Fig. 2 are turned on/off. In the zero link current state, the current is contained in the loop consisting of the link buffer inductor current Lb, switch Sb and diode Db, while the main thyristors switches TAx and TBx in Figure 1 are off. The link current is brought up to non-zero state by the turning on of the switch Si and thyristor Tr and turning of the switch Sb, followed by the firing of the main thyristors. This switching sequence along with carefully designed switching time creates several stages of multi resonant circuit modes that ensures the zero voltage or current switching (ZVS/ZCS) conditions of all the switches. Similarly, when the time comes to bring down the link current to zero state, switch Si is turned off and Sb is on following the firing of thyristor Tt that starts the termination process. Details of operation and design criteria for the link current generator shown in Fig. 2 can be found in [1].

A dedicated controller that provides the timing and decisions as when to turn on/off the switches is needed to control the operation of the switches in the link current generator. A good choice for this controller is a Field Programmable Gate Array (FPGA) which has also been used in this research. Some of the switches are turned on/off based on the timer event in the FPGA and some of them are controlled based on the conditions that occur in the circuit [1].

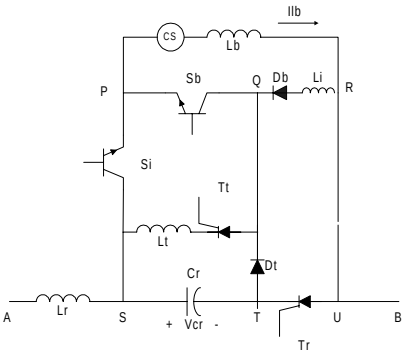

Fig. 2 Link Current Generator [1]

2.2 Power Transfer Control

Power transfer from the input to the output is controlled by selecting the combinations of the input and output main thyristor switches, which will be referred to here, as the input matrix and output matrix respectively. At each time, only two switches residing on different legs of each matrix can be selected. The thick lines in Fig. 1, for example, shows flow of the current in the converter when TA1 and TA4 are selected on the input, and TB3 and TB6 are selected on the output.

In the virtual test bed, a TMS320C50 Digital Signal Processor (DSP) has been used to implement the control algorithm for the input and output matrix selection to achieve the desired power transfer control objectives. In this research, the converter shown in Fig. 1 is intended to be used as a three-phase line conditioner with the following power transfer objectives:

1. Good output voltage regulation and low total harmonic distortion.
2. Near unity input power factor

Below, the output and input control algorithm that can be used to achieve these objectives are described.

A. Output Control

As can be seen from Fig. 1, the effect of the link current flow at the output is to charge and discharge one of the output filter capacitor C_B. With TB1 and TB4 selected, the capacitor voltage V_{UV} (which is also one of the output line voltages) is decreased since the capacitor is discharged with the link current flowing from V to U. If the TB2 and TB3 are selected instead of TB1 and TB4, the capacitor voltage V_{UV} will increase since now it is charged from the positive direction (U to V). The same principle applies for the line to line voltages VW and WU. For example to increase the output line voltage V_{VW} , we select TB4 and TB5, to decrease it we select TB3 and TB6. For V_{WU}, we use the combination of TB6 and TB1 or TB2 and TB5 to increase or decrease the voltage respectively.

It can be seen that the output matrix selection provides us with a way to control the output line voltages. For a multiphase application, like the one shown in Fig. 1, a Largest Error Algorithm [1] can be used to choose which line voltages need to be selected in order for the output to follow certain reference voltages. In this algorithm, the decision on which phase should be corrected at particular instant of time is based on the error between the actual line voltage and the reference voltages i.e. the phase with the largest error is the one to be corrected. The matrix selection can then performed by observing the sign of the error. Fig. 3 shows a block diagram of this algorithm.

Reference voltages used for the output depend on the intended applications of the converter. For variable frequency motor drive applications, for example, the reference voltages can be of variable magnitude and frequency based on the real time motor control requirement. For three phase line conditioner applications, the reference voltages consist of three phase balanced sine waves.

B. Input Control.

There are two objectives that need to be simultaneously achieved by the input control:

1. Controlling the input current to achieve near unity power factor
2. Maintaining sufficient link current to satisfy the output power demand

These two requirements can be achieved simultaneously by specifying input current references to be proportional to the input line voltages (ABC nodes in Fig. 1) with a proportional gain that is determined by the required link current. Denoting the proportional gain as *ILBREG*, the input current references are given by :

$$I_{ab(ref)} = V_{ab} \times ILBREG \quad \textbf{(1.a)}$$

$$I_{bc(ref)} = V_{bc} \times ILBREG \quad \textbf{(1.b)}$$

$$I_{ca(ref)} = V_{ca} \times ILBREG \quad \textbf{(1.c)}$$

Using these references, a similar largest error algorithm as in the output can be used. Fig. 4 illustrates the input error calculations. The block ILB Regulator in Fig. 4 computes the required link buffer current based on the power demanded by the output and generates the ILBREG gain for the references. The input error signals are then computed by taking the differences of the input currents and its derivatives with the reference currents. The input currents and their derivatives act as feedback PD Controllers that smooth out the current responses. Note that, these derivative terms are obtained from the voltages across the input inductors L_m (i.e differences between the input line currents and input capacitor voltages).

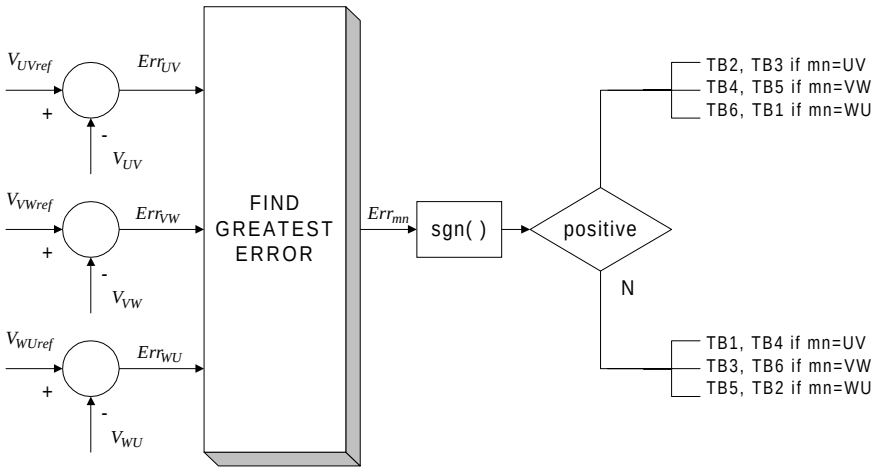

Fig. 3 Largest Error Algorithm for Output Matrix Selection

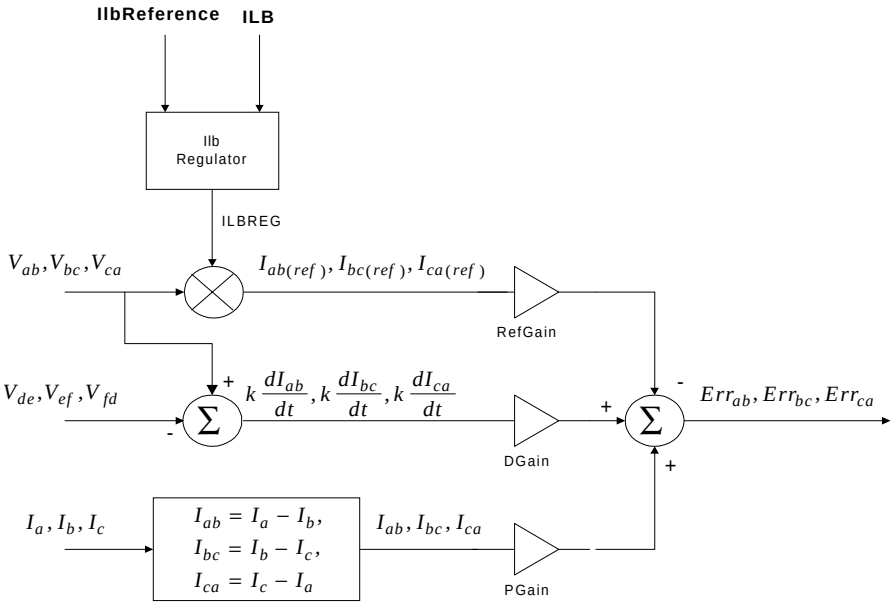

Fig. 4. Input Error calculations

C. Link Current Regulator (Ilb Regulator)

The functions of the Ilb Regulator are to maintain sufficient link current to satisfy the output power demanded by the load. As mentioned previously the Ilb Regulator produces the ILBREG gain that multiplies the input line voltages to obtain the current references. Fig. 5 shows the implementation of the Ilb Regulator. The error between the reference *ILBReference* and the actual *ILB* is fed to a PI Controller with anti-windup integrator which is realized as shown in Fig. 5.

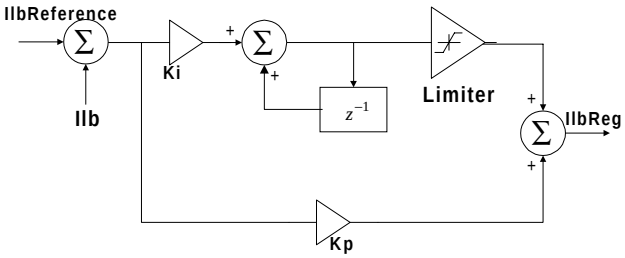

Fig. 5. Ilb PI Controller with anti-windup

III. THE OBJECT ORIENTED TEST BED SYSTEM

3.1. System Description

The virtual test bed system consists of a combination of a Windows 95/NT based software running on a PC with a TMS320C50 DSP controller board embedded on it as shown in Fig. 6. The Windows software performs the circuit simulation of the resonance converter and communicates with the DSP controller board that executes the user control codes.

Communication between the simulation software and the DSP controller board is performed through a dual access 16 bit digital I/O port as shown in Fig. 7. The user control codes are downloaded in to the on board RAM in the DSP control board or optionally executed on the TI's EPROM emulator.

3.2. Object Oriented Design and Implementation

The virtual test bed system is designed using Object Oriented approach and implemented using C++ programming language. Using the object oriented approach, the software system is first decomposed into objects that represent the actual hardware implementation as shown in Fig. 8. These objects are then further decomposed into each individual component building block and implemented as classes in C++ terminology.

The controller object consists of the DSP controller object and the FPGA object. The User Interface objects consist of a collection of objects such as scopes, waveform analyzer, and other graphical user interface objects. The Circuit object implements the resonance circuit simulation. A Global timer object is created to control the simulation timing of the virtual test bed system.

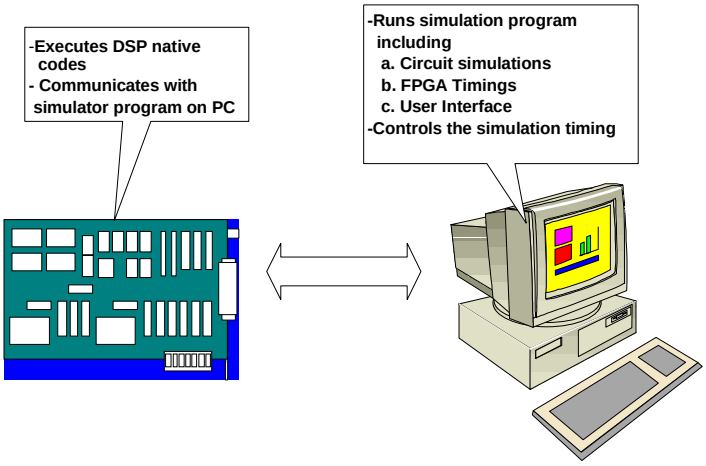

Fig. 6 Test Bed System

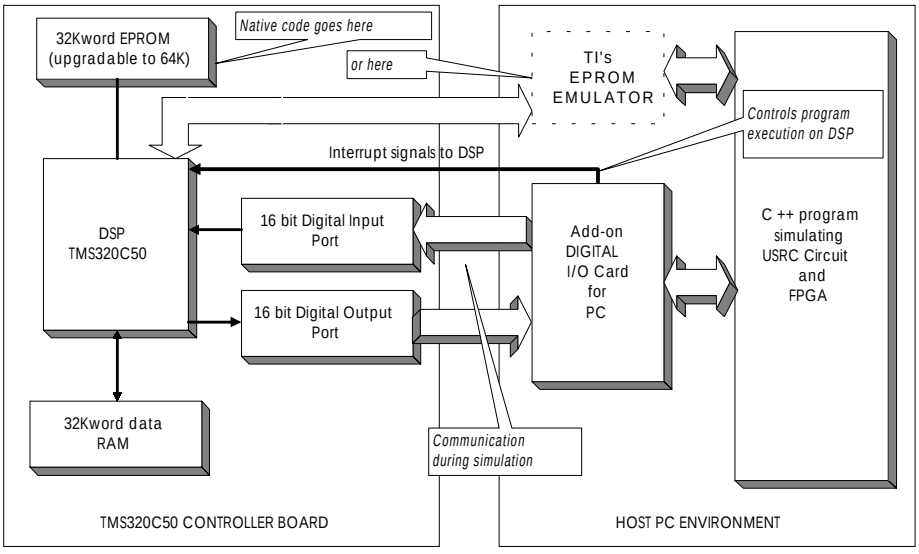

Fig. 7 Block Diagram of the Virtual Test Bed

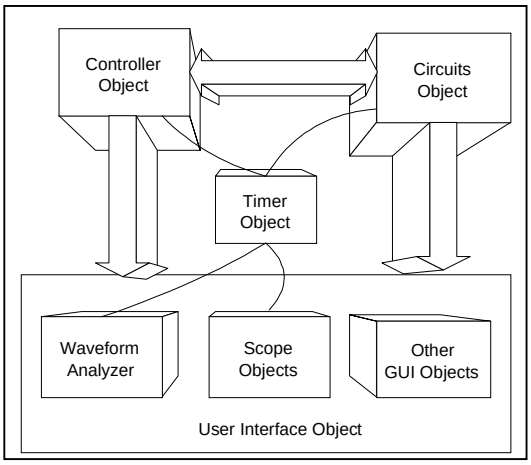

Fig. 8. Virtual Test Bed objects

IV. VIRTUAL TEST BED AND EXPERIMENTAL RESULTS

A hardware prototype of the unipolar series resonant converter has been built in the laboratory and the results are compared with those of the virtual test bed. The same component values and control algorithm have been used for both cases.

Fig. 9 and Fig. 10 show the virtual test bed plots of the input phase-phase currents and the output voltages respectively for the largest error algorithm at 1 p.u load. The input current distortion obtained using the largest error algorithm is 5-6% and the output voltage has a total harmonic distortion of 3%-4%. Fig. 11 and Fig. 12 show the results of the actual hardware implementation under the same load condition. It can be seen that the virtual test bed results match those of the actual hardware implementation.

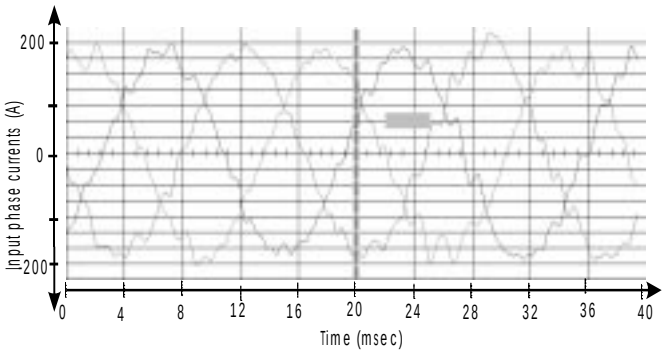

Fig. 9. Virtual test bed plot of line currents

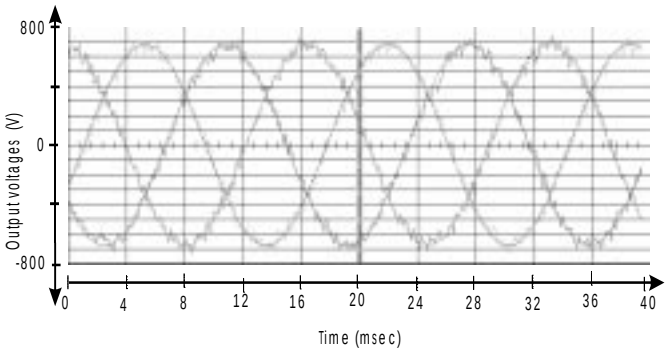

Fig. 10 Virtual test bed plot of output voltages

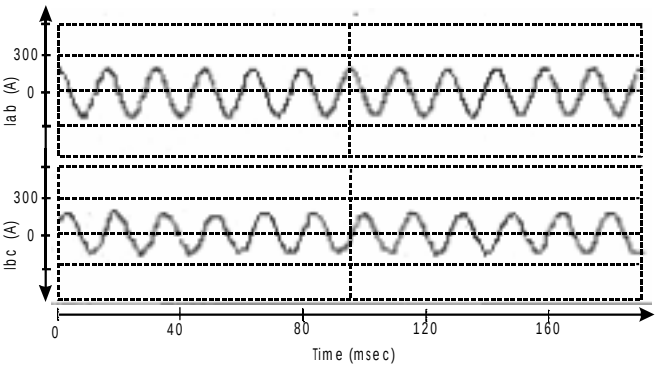

Fig. 11. Experimental input currents

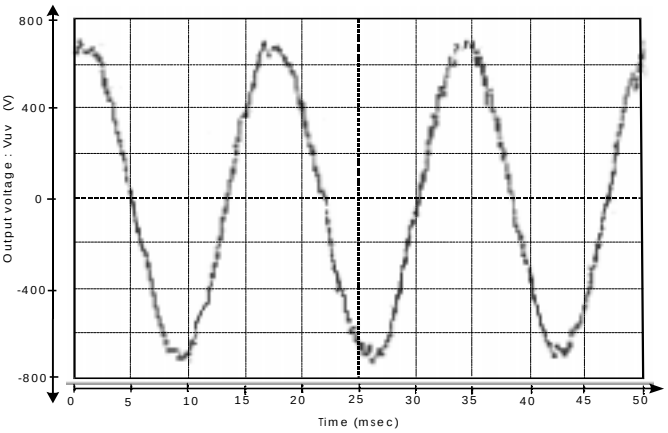

Fig. 12. Experimental output voltages

Fig. 13 and Fig. 14 show the plots of Cr capacitor voltage and the link current obtained from the virtual test bed and the experimental case. It can be seen that the virtual test bed yields results, which are very close to the actual hardware implementation. This proves that the circuit model approximation made in the virtual test bed is sufficient for evaluating the performance of the control algorithm.

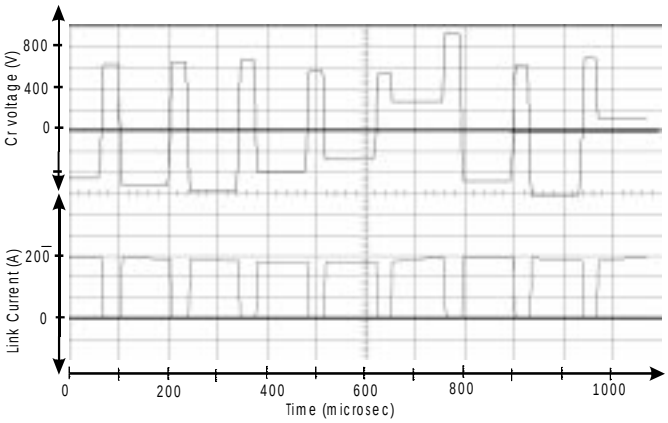

Fig. 13 Virtual test bed results : Cr capacitor voltage and link current

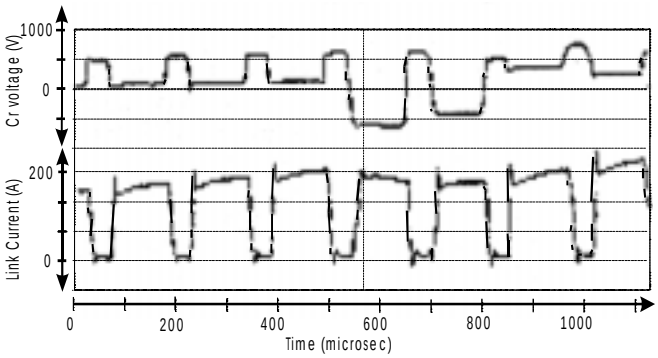

Fig. 14. Experimental link capacitor voltages and link currents

V CONCLUSIONS

In this paper, development of a virtual test bed for the design and control of a series resonant converter has been described. It was shown that the custom C++ software for the virtual test bed offers several advantages over the general simulation packages. Concept introduced in this paper can also be applied for different types of resonant converters and other power electronic systems.

VI ACKNOWLEDGMENT

This work is supported in part by National Science Foundation Grant No. 732884 and the Delphi Automotive System

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VIII BIOGRAPHIES

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