

## Problems Q1

1.[10 points] Find the shortest sequence of MIPS instructions to determine the absolute value of a two's complement integer. Convert this instructions:

abs \$t2, \$t3

This instruction means that register \$t2 has a copy of register \$t3 if register \$t3 is positive and the two's complement of register \$t3 if \$t3 is negative.

### Solution

```
addu $t2, $zero, $t3 # copy $t3 into $t2
bgez $t3, next      # if $t3 >= 0 then done
sub $t2, $zero, $t3 # negate $t3 and place into $t2
```

Next:

3. [6 points] Decode the following as both signed and unsigned numbers:

00001011  
01011011  
11110100

### Solution

00001011 Signed =  $(8+2+1) = 11$

Unsigned =  $(8+2+1) = 11$

01011011 Signed =  $(64+16+8+2+1) = 91$

Unsigned =  $(64+16+8+2+1) = 91$

11110100 Signed =  $-(8+4) = -12$

Unsigned =  $(128+64+32+16+4) = 244$

4. [8 points] Given the bit pattern:  
1010 1101 0001 0000 0000 0000 0000 0010

What does it represent, assuming that it is:

a) a two's complement integer?

a. -1 391 460 350

b) an unsigned integer?

b. 2 903 506 946

c) a single precision floating-point number?

c.  $-8.18545 \cdot 10^{-12}$

d) a MIPS instruction?

Sw \$s0, \$t0(16) sw \$r16, \$r8(2)

5. [10 points] Consider two different implementations, P1 and P2 of the same instruction set. There are five classes of instructions (A, B, C, D and E) in the instruction set. P1 has a clock rate of 4GHz. P2 has a clock rate of 6 GHz. The average number of cycles for each instruction class for P1 and P2 is as follows:

Class	CPI on P1	CPI on P2
A	1	2
B	2	2
C	3	2
D	4	4
E	3	4

Compare the peak performance.

If the number of instructions executed in a certain program is divided equally among the classes of instructions except for class A, which occurs twice as often as each of the others, how faster is P2 than P1?

The ideal instruction sequence for P1 is one composed entirely of instructions

from class A (which have CPI of 1). So M1's peak performance is  $(4 \times 10^9 \text{ cycles/second}) / (1 \text{ cycle/instruction}) = 4000 \text{ MIPS}$ .

Similarly, the ideal sequence for M2 contains only instructions from A, B, and C (which all have a CPI of 2). So M2's peak performance is  $(6 \times 10^9 \text{ cycles/second}) / (2 \text{ cycles/instruction}) = 3000 \text{ MIPS}$ .

The average CPI of P1 is  $(1 \times 2 + 2 + 3 + 4 + 3) / 6 = 7/3$ . The average CPI of P2 is  $(2 \times 2 + 2 + 2 + 4 + 4) / 6 = 8/3$ . P2 then is  $((6 \times 10^9 \text{ cycles/second}) / (8/3 \text{ cycles/instruction})) / ((4 \times 10^9 \text{ cycles/second}) / (7/3 \text{ cycles/instruction})) = 21/16$  times faster than P1.

6. [5 points]

Design (read part only) a typical organization (i.e. two level decoding design) of  $32\text{K} \times 8$  SRAM chip that uses  $512 \times 64$  arrays of D-latches.

$$512 \times 64 = 32768 = 32\text{K}$$

7. [10 points]

Minimize using Karnaugh Maps

X1	X2	X3	O
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

		X1X2			
		00	01	10	11
X3	0	1	1	1	0
	1	1	0	1	0

$$O = \overline{X1}X2 + X1\overline{X2} + \overline{X1}X3$$

7. Multi choice and True or false? (Grading: +1 for each correct answer. -1 for each incorrect answer. 0 for no answer)

1. For a given instruction set architecture, increases in CPU performance can come from \_\_\_\_\_
  - a) Increases in clock rate.
  - b) Improvement in processor organizations the lower the CPI.
  - c) Compiler enhancements that lower the instruction counter
2. Compilers affect \_\_\_\_\_
  - a) Instruction count
  - b) Clock rate
  - c) CPI

**T F**

3.   CPU is the active part of the computer, following the instructions of a program to the letter.
4.   Datapath is the component of the processor that performs arithmetic operations.
- 5   Assembler is the program that manages the resources of a computer for the benefit of the programs that run on that machine.
- 6   Compiler is the program that translates from a high-level notation to assembly language.
7.   Instruction format is a form of representation of an instruction composed of fields of binary numbers.
8.   shamt is the field that denotes the operation and format of an instruction.
9.   Execution time is the only valid and unimpeachable measure of performance.
10.   Through the use of weights, a weighted arithmetic mean can adjust for different running times, balancing the contribution of each benchmark to the summary.
11.   MIPS is a measurement of program execution speed based on the floating point operations.
12.   Expecting the improvement of one aspect of a computer to increase performance by an amount proportional to the size of the improvement.
13.   The fastest computer will be always the one with the highest clock rate.
14.   Weighted arithmetic mean is the average of the execution time that is directly proportional to the total execution time.