## CS 3501: Computer Organization and Design

## Mid Term Examination (03/06/08)

1. This is a CLOSED book exam.
2. No questions will be answered in class. Make any assumptions you want to make, and write down the assumptions in the exam.
3. Read every question carefully and completely. You have to answer all parts of a question to receive full grade.
4. Make sure you have written down your name and email on the top right corner of this page.

Time: 1:40pm - 3:00pm, March 06, 2008
Number of questions: questions
Total Points: 100
\% of final grade: 30
Q. 1 [10 points]

Describe the definition of the Von Neumann Model and explain whether ENIAC used the Von Neumann Model.

Stored-program computers have become known as von Neumann Architecture systems.
On the ENIAC, all programming was done at the digital logic level.
Programming the computer involved moving plugs and wires.
A different hardware configuration was needed to solve every unique problem type.
So Eniac used non von Neumann model.
Q. 2 [10 points]
(a) Describe benefit of 1's complement number compared with signed magnitude representation

1's Complement systems are useful because they eliminate the need for different subtraction. simpler addition without subtraction
(b) Describe benefit of 2's complement number compared with 1's complement number representation.

- only one representation for zero
(c) Represent -3 using signed binary magnitude representation (8 bits)

10000011
(d) Represent -3 using 1’s complement binary number representation (8 bits)

11111100
(e) Represent -3 using 2's complement binary number representation (8 bits)

11111101

## Q. 3 [10 points]

Express negative floating point decimal number, $-26.625_{10}$, in the 14-bit floating point model which consists of 1 sign bit and 5 bits of exponent and 8 bits of significand. Exponent field uses 16 biased exponent.

Q. 4 [20 points]
(A) [10points] Assume that you have the following sum of product form of a function. Fill out the truth table based on the following sum of product form.
$\mathrm{F}(\mathrm{w}, \mathrm{x}, \mathrm{y}, \mathrm{z})=\overline{w x y z}+\overline{w x y} \bar{z}+\bar{w} x \bar{y} z+\bar{w} x y z+\bar{w} x y \bar{z}+w \overline{x y z}+w \bar{x} y \bar{z}$

| Input: wxyz | Output: F |  |
| :---: | :---: | :--- |
| 0000 | 1 |  |
| 0001 | 0 |  |
| 0010 | 1 |  |
| 0011 | 0 |  |
| 0100 | 0 |  |
| 0101 | 1 |  |
| 0110 | 1 |  |
| 0111 | 1 |  |
| 1000 | 1 |  |
| 1001 | 0 |  |
| 1010 | 1 |  |
| 1011 | 0 |  |
| 1100 | 0 |  |
| 1101 | 0 |  |
| 1110 | 0 |  |
| 1111 | 0 |  |
|  |  |  |

(B) $[10$ point $]$

Create the Kmaps based on the above $\mathrm{F}(\mathrm{w}, \mathrm{x}, \mathrm{y}, \mathrm{z})$ and then simplify the $\mathrm{F}(\mathrm{w}, \mathrm{x}, \mathrm{y}, \mathrm{z})$ function.


X'Z' + W'XZ + W'XY
Q. 5 [10 points]

Explain the drawback of the ripple carry full adder when you need to design 64-bit CPU core. And give a solution for the drawback. (Just give a name of the circuit. You don't need to draw a circuit of solution)

Carry-look ahead adder

## Q. 6 [10 points]

Assume that you need to design the control circuit for an interrupt handler which handles up to four different kinds of simultaneous interrupts at the same time based on different priority of interrupts. Give a name of a common circuit which you need to build the control circuit.
And draw a truth table which has four different input variables (D1, D2, D3, D4) and two different output variables (A0, A1).

Priority Encoder

| Inputs |  |  |  |
| :---: | :---: | :---: | :---: |
| $\mathbf{D}_{3}$ | $\mathbf{D}_{2}$ | $\mathbf{D}_{1}$ | $\mathbf{D}_{0}$ |
|  |  |  |  |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | X |
| 0 | 1 | X | X |
| 1 | X | X | X |


|  | Outputs |
| :---: | :---: |
| $\mathbf{A}_{\mathbf{1}}$ | $\mathbf{A}_{\mathbf{0}}$ |
|  |  |
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 1 | 1 |

Q7. [10 points]
Fill out the following truth tables for SR latch and JK flip flop

| S |  | R |
| :---: | :--- | :--- |
| 0 | 0 | $\mathrm{Q}(\mathrm{t})$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | undefined |


| J |  | K |
| :--- | :--- | :--- |
| 0 | 0 | $\mathrm{Q}(\mathrm{t})$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\mathrm{Q}^{\prime}(\mathrm{t}+1)$ |

Q8. [10 points]
A Digital computer has a memory unit with 32 bits per word. The instruction set consists of 260 different operations. All instructions have an operation code part (opcode) and an address part (allowing for only one address). Each instruction is stored in one word of memory.
a) How many bits are needed for the opcode ?

2^9 > 260
So 9 bits for opcode
b) How many bits are left for the address part of the instruction ?

23 bits
c) What is the maximum allowable size for memory ?
$2^{\wedge} 23$
d) What is the largest unsigned binary number that can be accommodated in one word of memory ?
$2^{\wedge} 32-1$

