Computer Architecture
(CSC-3501)
Lecture 8
(12 Feb 2008)

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Announcement
4-Bit Register (Sequential Circuits)

- This illustration shows a 4-bit register consisting of D flip-flops. You will usually see its block diagram (below) instead.

![Register Diagram]

4 X 3 Memory

- 3 bit input
- $2^3$ memory selection
- 2 words selected by $S_0$ and $S_1$
4-Bit Synchronous Counter

- A binary counter is another example of a sequential circuit.
- The low-order bit is complemented at each clock pulse.
- Whenever it changes from 0 to 1, the next bit is complemented, and so on through the other flip-flops.

Finite State Machines

- The behavior of sequential circuits can be expressed using characteristic tables or finite state machines (FSMs).
  - FSMs consist of a set of nodes that hold the states of the machine and a set of arcs that connect the states.
- Moore and Mealy machines are two types of FSMs that are equivalent.
  - They differ only in how they express the outputs of the machine.
- Moore machines place outputs on each node, while Mealy machines present their outputs on the transitions.
Moore vs. Mealy

- The behavior of a JK flop-flop is depicted below by a Moore machine (left) and a Mealy machine (right).
- Although the behavior of Moore and Mealy machines is identical, their implementations differ.

Moore Machine

- J-K Flip Flop

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q(t) (no change)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0 (reset to 0)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1 (set to 1)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>~Q(t)</td>
</tr>
</tbody>
</table>

Combination Logic → Sequential Logic (Memory) → Combinational Logic → Output
Mealy Machine